A Dielectric-Defined Process for the Formation of *T*-Gate Field-Effect Transistors

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Abstract—**A novel process for the fabrication of Tee- or Gamma-shaped gate structures is presented. This process was utilized to fabricate 0.25 μm × 60 μm and 0.25 μm × 150 μm *T*-gate MESFET's. From *s*-parameter data up to 40 GHz, extrapolated cut-off frequencies (f_t,) as high as 55–65 GHz were obtained. This represents some of the highest f_t's ever reported for a MESFET. DC yields as high as 80% over 3″ wafers, were obtained using this dielectric defined *T*-gate (DDTG) process. Further, step-stress measurements indicate device reliability comparable to our normal MESFET process. Relative to multilayer resist processing techniques usually employed to form *T*-gates, we believe the DDTG process will substantially increase the yield, uniformity and reliability of FET-like devices/circuits employing *T*-gates with geometries at or below 0.25 μm.**

I. Introduction

It is well known that at millimeter-wave frequencies, gate resistance (R_g) is one of the dominant device parasitic elements limiting MESFET (metal semiconductor field effect transistor) and HEMT (high electron mobility transistor) circuit performance. Because of skin effects, as the operating frequency increases into the millimeter-wave, gate resistance values increase dramatically and have even been reported to be as high as 2,200 ohm–mm [1]. Clearly, such high gate resistance values will utlimately affect MMIC RF performance, such as increasing amplifier noise figure or reducing gain.

In an attempt to reduce the detrimental problems associated with the skin effect, numerous laboratories have proposed and demonstrated various techniques to produce the so-called Tee or mushroom-shaped gate. Historically, most, if not all, approaches to form the *T*-gate structure have utilized a multiresist technique. In the multiresist process, the engineer relies on the different resist sensitivities to replicate the desired *T*-gate profile. More often than not, however, this approach is not highly reproducible and offers less degree of flexibility in achieving the desired *T*-gate profile and/or aspect ratio (e.g., ratio of top gate dimension to gate length). Furthermore, achieving uniform device passivation under the overhang of the *T*-gate, and/or shorting of the wide aspect ratio gates to either the source or drain ohmic, in offset or narrow channel devices, are two additional problems associated with the multiresist approach that can limit reliability and yield.

In this letter, we will present an alternative technique [2] that we believe is superior in almost every respect to the aforementioned multilevel resist approach to forming high aspect ratio gate structures.

II. Material Growth and Device Fabrication

The MESFET structures used in this work were grown in a RIBER molecular beam epitaxy system. The MESFET material structure was as follows: 1) 5000 Å of undoped GaAs were grown on top of the semi-insulating, 3″ GaAs substrate; 2) 500 Å of undoped GaAs, 2000 Å of GaAl–AlGaAs undoped superlattice and 2000 Å of undoped GaAs were grown to served as the buffer layer; 3) 1000 Å of GaAs doped to 5×10^{17} cm^{-3} was grown for the active channel layer, and finally; 4) 300 Å of 6×10^{18} cm^{-3} GaAs was grown for the ohmic cap layer.

The first step in the DDTG process begins with the plasma-enhanced chemical vapor deposition (PECVD) of 1000 Å of Si_3N_4 on top of the exposed n^+ GaAs (Fig. 1(a)). PMMA is next spun on and the wafer *e*-beam exposed and developed to produce the 0.25-μm opening in the PMMA. The exposed Si_3N_4 is then etched away in a reactive ion etching (RIE) apparatus using SF_6 as the reactive gas (Fig. 1(b)). A slight 10 second "over etch" is performed to insure complete and uniform opening of the nitride. The dry etching conditions (e.g., pressure, voltage, etc.) were adjusted to minimize surface damage to the n^+ GaAs. Nevertheless, any damage that does exist will be remove during the wet chemical etching of the recessed gate notch. Further, because this dry etching process is highly anisotropic, little or no lateral side-wall etching of the nitride was observed (even with the 10 second over etch). Once the nitride is opened, the wafer is cleaned and re-coated with new PMMA/photo-resist. The wafer can now be *e*-beam or optically exposed to produce the desired gate-top profile (Fig. 1(c)). Because the exposure dosage and/or method used for the *T*-gate footprint is completely independent from the exposure dosage and/or method used to form the top portion of the gate, very large aspect ratio *T*-gates can be obtained (Fig. 2). Since the top portion of the gate can be almost any dimension, this second step in the gate lithography can be done using conventional optical mask aligners. Additionally, since the dimension between the bottom of the gate overhang and the top of the GaAs surface is defined by the thickness of the nitride, a very thin layer of PMMA (e.g., < 1000 Å) can be used in the first step of the

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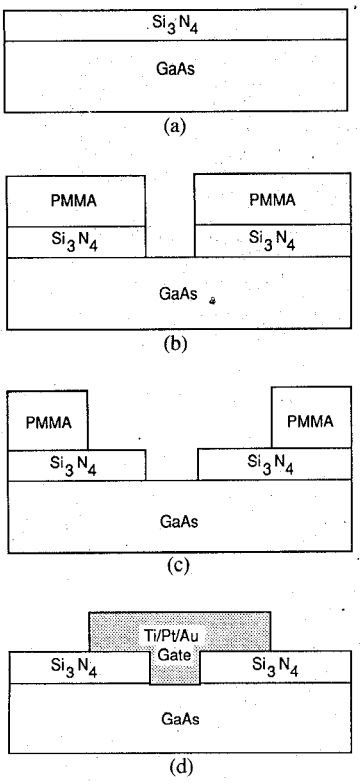

Fig. 1. Dielectrically defined *T*-gate (DDTG) process steps. (a) PECVD deposition of nitride. (b) RIE formation of gate foot print. (c) Second resist layer formation of top of *T*-gate. (d) Channel recess and gate metal deposition.

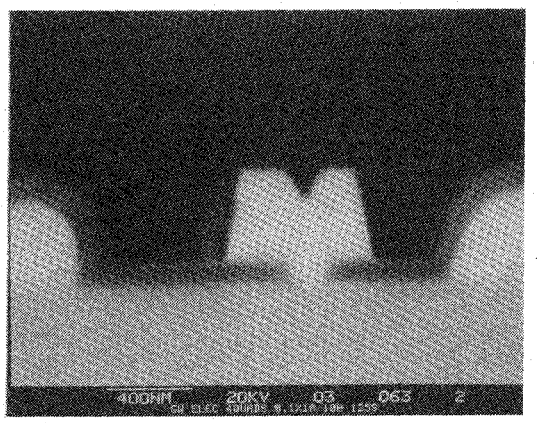

Fig. 2. Cross-sectional SEM photograph of 0.25-μm DDTG.

DDTG process. Reducing the thickness of this PMMA layer significantly improves the probability of reproducing sub-0.25-μm openings in the PMMA. Finally, the gate recess notch is formed by placing the wafer in a spray etching apparatus. The gate etching solution is citric acid-based. Approximately 300 Å of n^+ GaAs is etched away, thus removing any material that may have been damaged during the RIE process. Further, since we are only etching down approximately 300 Å, there is little side etching of the GaAs. The final *T*-gate structure, after the Ti–Pt–Au gates have been formed using standard lift-off procedures, is shown in Fig. 2.

III. DC and RF Results

After front-side is complete, the wafer was dc auto-probed to determine device yield and operating characteristics. Approximately 80% of the 0.25-μm *T*-Gate devices were found to be functional. Variations (σ/mean) in dc characteristics ranged from a low of 12% for I_{dss} to a high of 20% for $G_{m,\,max}$. This percentage variation is typical for such highly doped (i.e., 5×10^{17} cm^{-3}) material. One would expect variation of only 5–10% for samples doped to $1\text{–}2 \times 10^{17}$ cm^{-3}. Nevertheless, the aforementioned uniformity and yield statistics were found to be considerably better than other in-housed processed 0.25-μm *T*-gate wafers that used the conventional double-level resist process. Most DDTG processed devices were found to have transconductance values of 300–350 mS/mm, $V_{br} \sim 8$ v, $V_p \sim -0.8$ and $I_{dss} \sim 150$ mA/mm. The transfer characteristics (i.e., I_{ds} and G_m) for a typical 0.25 μm $\times$ 150 μm DDTG device is shown in the insert of Fig. 3.

S-parameter measurements, up to 40 GHz, were performed on several 0.25 μm $\times$ 150 μm DDTG MESFET's selected at random. Shown in Fig. 3 are the plots of H_{21} and MSG/MAG versus frequency for a typical device biased near peak G_m (see Fig. 3 insert)[1]. Extrapolating H_{21} to zero gain, an estimate of 58 GHz is made for the cut-off frequency (f_t). We believe this to be one of the highest cut-off frequencies ever reported for a 0.25-μm MESFET. Furthermore, the stability factor, k, had values considerably less than one up to and including 40 GHz. This would also account for the lack of inflection points in the data shown in Fig. 3. From the *s*-parameter measurements of the device of Fig. 3, an assessment of its equivalent circuit (under this bias condition) was made and is shown in Fig. 4. As expected, the normalized gate resistance is about a factor of 10 times smaller than what we would normally obtain for a rectangular 0.25-μm gate-length device. Finally, step-stress measurements were performed on 30 DDTG MESFET's to determine if this process presented any reliability problems. Indications are that the DDTG MESFET's are as reliable as normally processed 0.25-μm MESFET's, with a mean-time-to-failure in excess of 10^6 hours at a channel temperature of 100 C.

IV. Conclusion

We have presented an alternative technology to the formation of *T*-gate structures for millimeter-wave devices. It is our belief that the DDTG process is superior to the conventional multilayer resist process because it inherently decouples the formation of the small gate foot-print from the much larger top portion of the gate, and as such, sub-0.25-μm gates with very large aspect ratios can be routinely and repro-

[1] As a point of interest, plots of H_{21} and MSG/MAG were made from the *s*-parameter calculations of both TOUCHSTONE™ from EESOF and MICROCAT™ software from CASCADE. Shown in Fig. 3 are the more conservative results of the TOUCHSTONE™ program, which are consistent with well known *s*-to-*h* matrices conversion equations. To our surprise, however, the MICROCAT™ calculations for H_{21} were as much as several dB higher than those from TOUCHSTONE™. In fact, using the output from MICROCAT™ gave an extrapolated value for f_t of approximately 70 GHz (instead of 58 GHz). As of now, we have not resolved this discrepancy. We thought your readers might appreciate knowing of this discrepency.

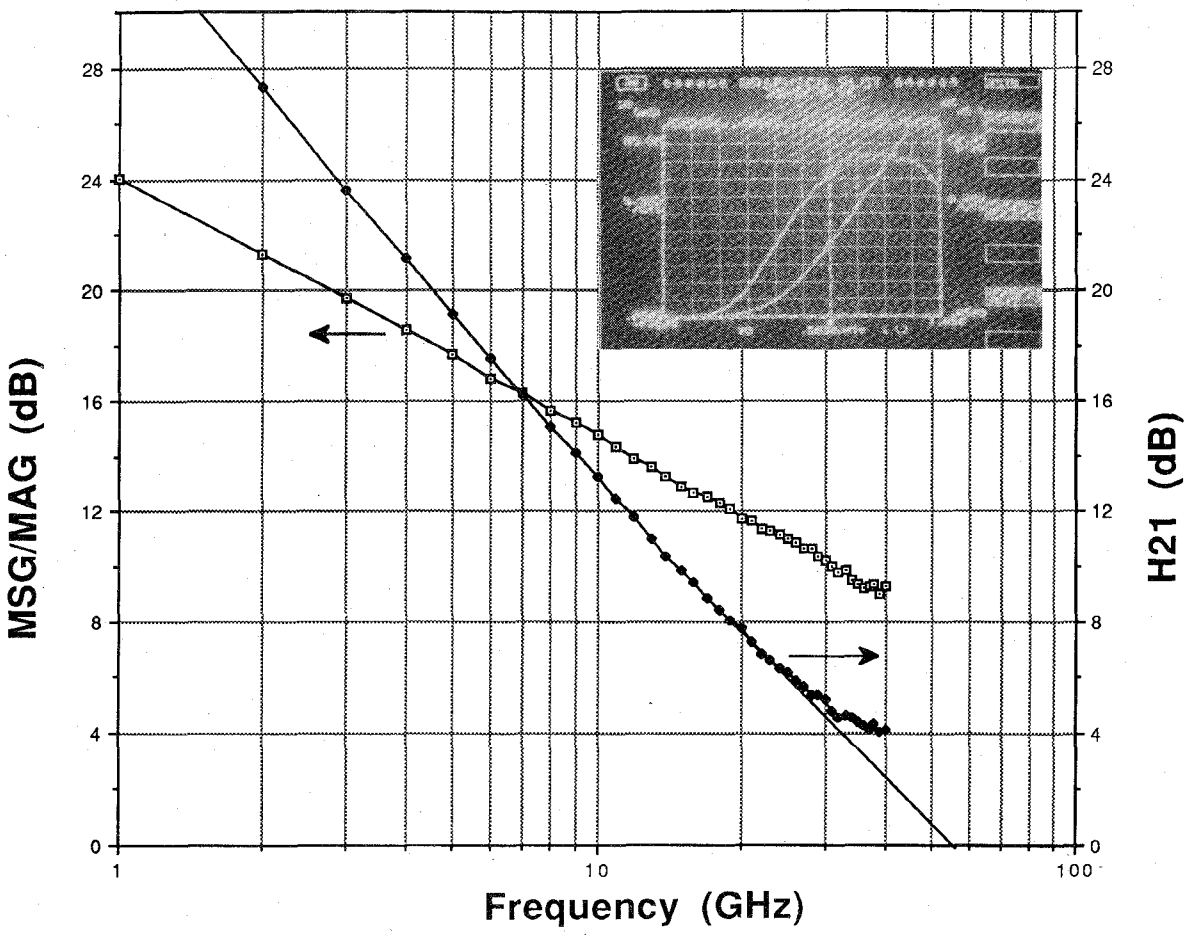

Fig. 3. Plot of H_{21} and MAG/MSG versus frequency for a typical 025-μm DDTG MESFET. Bias conditions: V_g = 0.3 v and V_{ds} = 2.5 v. Insert shows the I_{ds} and g_m transfer characteristics for this MESFET.

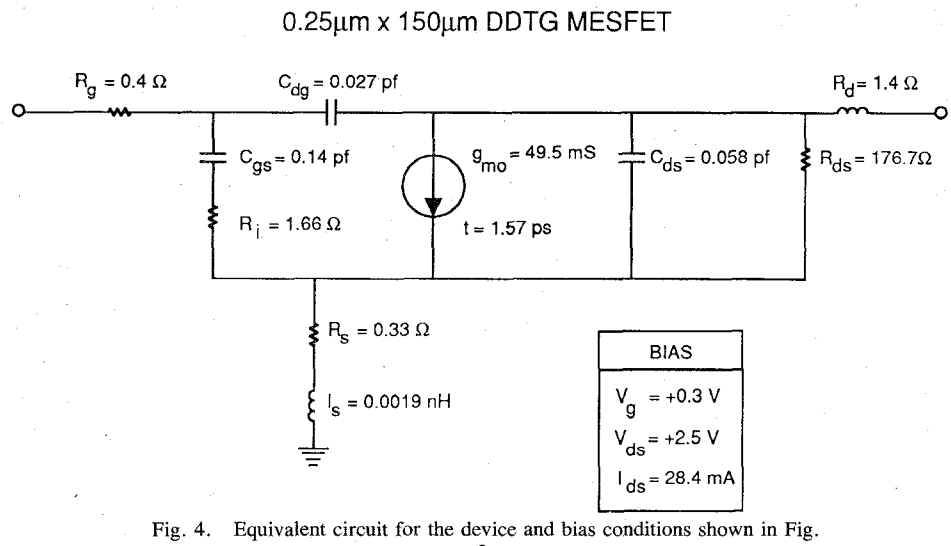

Fig. 4. Equivalent circuit for the device and bias conditions shown in Fig. 3.

ducibly obtained. Finally, we have used the DDTG process to fabricate discrete 0.25-μm gate-length MESFET's, which had yields as high as 80%, and state-of-the-art performance in both power and current gain.

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